Demonstration of 10-Gb/s, 5-GHz Spaced Coherent UDWDM-PON with Digital Signal Processing in Real-Time

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Abstract: This paper experimentally demonstrate the real-time field trial of 40×10-Gb/s coherent UDWDM-PON at 5-GHz spacing over 40-km field-installed fiber. The system stability is demonstrated by 8-hour real-time BER measurement with power budget of 29 dB.
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1. Introduction

Optical access networks based on coherent detection and ultra-dense wavelength-division multiplexing (UDWDM) technology have been demonstrated as potential candidate to increase the network capacity and the spectral efficiency [1, 2]. Although the complexity of digital coherent receiver is higher than conventional receiver in direct-detection scheme, the system will be benefitted due to the reduced operational costs per subscriber with increased channel capacity, which allow multiple subscribers sharing one single fiber. Several coherent UDWDM passive optical network (PON) schemes have been experimentally demonstrated in either off-line [3, 4] or real-time mode [5-7]. However, the data rate per channel is usually less than 5-Gb/s. As the demand for broadband applications continues rising, 10-Gb/s per channel is required in future UDWDM architectures.

In this paper, we demonstrate a real-time operation of dual-polarization quadrature phase shift keying (DP-QPSK)-based system for coherent UDWDM-PON. The digital signal processing (DSP) for optical line terminals (OLT) and optical network units (ONU) is achieved by field-programmable gate arrays (FPGAs). For experimental demonstration, a UDWDM-PON scheme is realized based on 40 channels and 10-Gb/s DP-QPSK signals spaced at 5 GHz over 40 km field-installed fiber. The bit error rate (BER) keeps below 3.8×10^{-3} for 10-Gb/s downstream signal per wavelength during a 8-hour real-time environment measurement with 29 dB loss budget. The successful demonstration will facilitate UDWDM-PON moving forward to practical deployment and applications.

2. Configuration of 40×10Gb/s UDWDM-PON

Fig. 1 shows the structure of the UDWDM-PON and the corresponding OLT and ONU sides for the downlink. In the OLT side, 40 external cavity lasers (ECL) (<100 kHz–linewidth) are used as odd and even channels at channel spacing of 10-GHz for channel de-correlation, respectively. The optical spectrum of 40 laser sources is shown in the inset (I) of Fig. 1. In the OLT side, the DP IQ modulator (DP-IQM) is driven by the electrical 2.5-Gb/s 2^{23}-1 pseudo random bit sequence (PRBS) from Altera Stratix V FPGA, which is working at 156.25 MHz and parallelization level of 16 to generate the digital QPSK signal. An electrical low-pass filter with bandwidth of 2 GHz is used to shape the spectrum of the generated QPSK signal to mitigate the channel interference. After electrical to optical conversion, the odd and even channels are combined by one optical coupler, which result in a UDWDM grid of 5 GHz. Two erbium doped fiber amplifiers (EDFA) are used for the respective odd and even channels to control the total transmitted optical power of 5 dBm for the 40 channels, corresponding to the launch power of -11 dBm for each channel.

The total optical signal is transmitted over 40 km field-installed fiber. The transmitted optical spectrum is shown in the inset (II) of Fig. 1. The bandwidth of the optical signal is 200 GHz with each subscriber occupying bandwidth of 5 GHz. In our experimental demonstration, a variable optical attenuator (VOA) is used to emulate the 1:40 passive optical splitter for the 40 subscribers. At the receiver side, the QPSK channels are selected by tuning another ECL local oscillator (LO) and coherently detected in an integrated coherent receiver (ICR). It is noted that there is no optical filter used at the ONU side which saves the cost of the PON system.

In the electrical domain at the ONU side, the signal is sampled by two 8-bit 5 GSa/s ADC with an analog bandwidth of ~2 GHz. The amplitude of the electrical signal is adjusted by appropriately setting the LO power and transimpedance amplifiers (TIA) in the ICR. After analog-to-digital conversion, the digitalized signal is sent to a Stratix V FPGA where all post-detection 8-bit DSP in real-time is implemented. After the clock recovery subsystem, the signal is down-sampled to preserve two samples per symbol for channel equalization and finally the carrier recovery is performed. The FPGA operating frequency is set to 156.25 MHz, leading to a parallelization level of 32

in order to enable real-time processing at 5 GSa/s. The bit error rate (BER) is estimated on a personal computer with respect to the transmitted PRBS. We integrate both the transmitter and receiver modules in one electrical board, where both upstream and downstream operations can be achieved as also shown in Fig. 1.

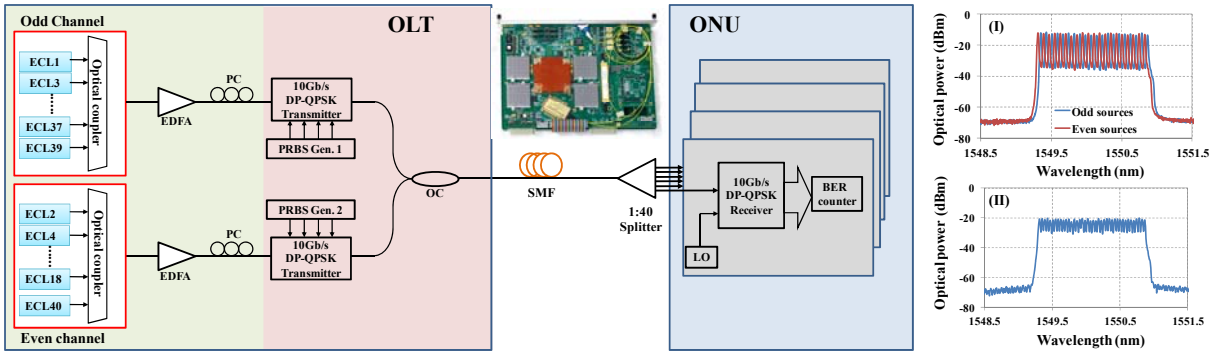


Fig. 1 Transmission scheme of 40×10Gb/s UDWDM-PON system including the pictures of OLT and ONU line cards for downlink. Inset: (I) optical spectrum of 40 optical sources at the OLT side; (II) optical spectrum of transmitted optical signals at the OLT side. OC: optical coupler. Gen: generator. LO: local oscillator.

3. DSP Architecture

In this section, we mainly consider the DSP architecture at the receiver side, which is shown in Fig. 2. After collecting the four-channel samples from the four ADCs, serial to parallel conversion is achieved in FPGA, where each channel has a parallelization level of 32 for clock recovery operation. Classical Gardner algorithm is used to minimize the output value θ_e, which is proportional to the value of phase deviation when sampling offset exists. After clock recovery, constant module algorithm based adaptive filtering is applied to achieve the channel dispersion compensation and polarization demultiplexing. In order to realize parallel computing in FPGA, 16 parallel streams in each polarization are calculated simultaneously to obtain 32 outputs for the signals in two polarizations. Two outputs are chosen to update the channel state matrix with tap number of 7 in our demonstrations. Finally, the differential phase-based method with a 32 symbol-tap and the Viterbi & Viterbi algorithm is used in the carrier phase recovery stage. The equalized complex signal will be converted to angle based on coordinate rotation digital computer (CORDIC) algorithm [8]. This technique has been shown effective and efficient for MPSK modulation formats, which only requires addition, subtraction, bitshift and table lookup operations inside the FPGA [9].

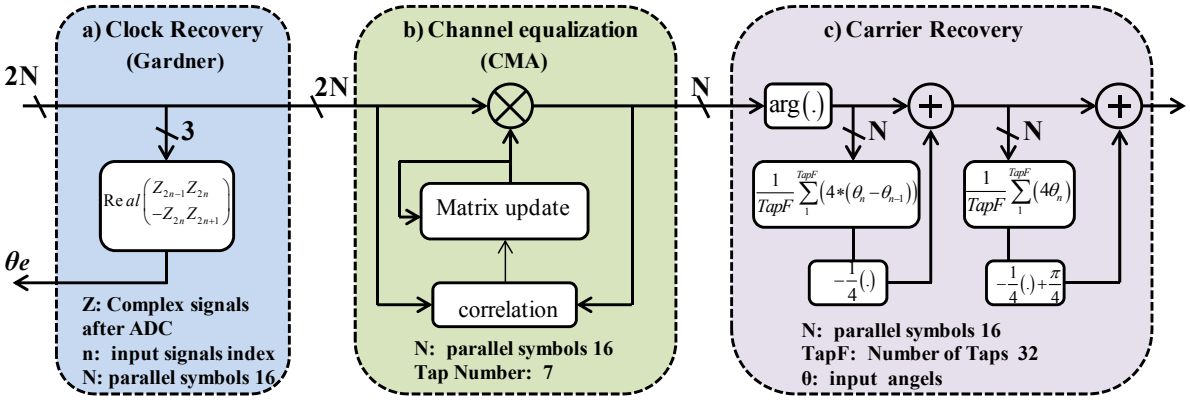


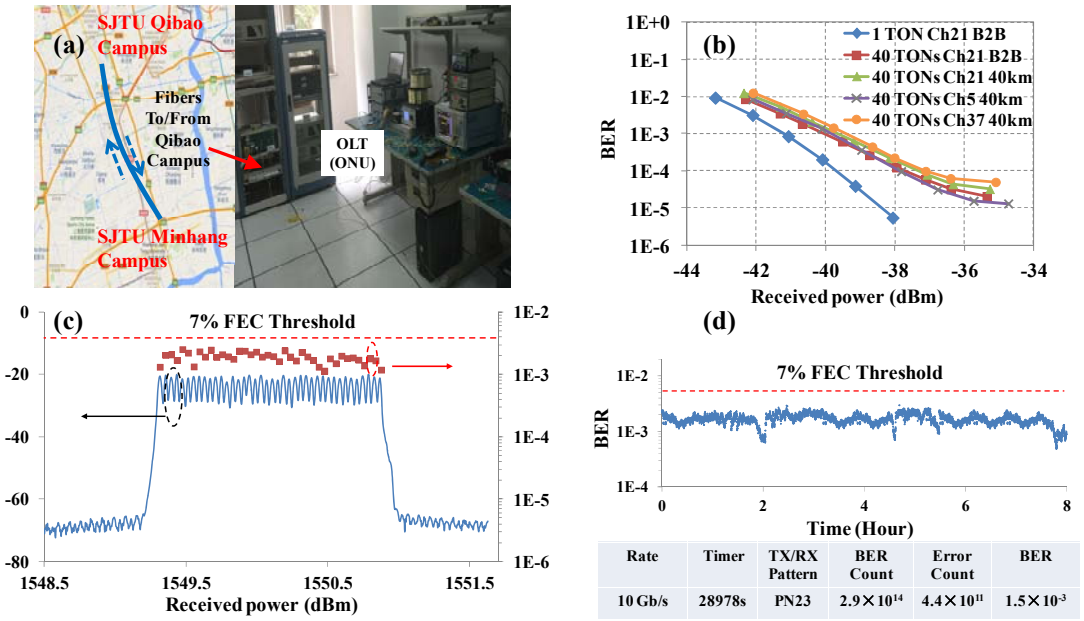
Fig. 2 DSP architecture in FPGA-based receivers(in ONU): (a) clock recovery; (b) channel equalization; (c) carrier recovery.

4. Experimental Results and Discussion

In the experimental demonstration, a round trip fiber link is chosen between Minhang campus and Qibao campus of Shanghai Jiaotong University (SJTU) with total fiber length of 40 km, as shown in Fig. 3(a). Both the OLT and ONU boards are located at Minhang campus. It is noted that the total loss of the system in the field demonstration is 18 dB due to the degraded field-installed fiber loss.

We first evaluate the BER performances of the 21st channel, as shown in Fig. 3(b). The receiver sensitivity can achieve -40 dBm at the 7% threshold of 3.8×10^{-3} for each channel when all the 40-channel optical signals are

transmitted over 40-km field-installed fiber. The transmission penalty is negligible when comparing with the back-to-back (B2B) case. It is also shown that in the B2B condition, the receiver sensitivity of single channel is 1 dB higher than that of 40 channels. The performance degradation is mainly caused by the strong nonlinear effects when all the 40-channel optical signals are converted into the electrical signals in one ICR. The BER versus receiver power for the 5th, 21st and 37th channels are also shown in Fig. 3(b), where the performances are similar for all the 3-channel optical signals. Then, we measure the BER performances for all the 40 optical channels at receiver power of -40 dBm for each channel. As shown in Fig. 3(c), all the 40-channel optical signals can achieve 7% FEC threshold. Finally, the BER performance of the 21st channel after ~8-hour real time measurements is shown in Fig. 3(d). The variation of BER along the 8-hour is small, and the average value of BER is 1.5×10^{-3}, well below the 7% threshold. Considering the launch power of -11 dBm per channel at the OLT side, the power budget is 29 dB in the field transmission.



Rate	Timer	TX/RX Pattern	BER Count	Error Count	BER
10 Gb/s	28978s	PN23	2.9×10^{14}	4.4×10^{11}	1.5×10^{-3}

Fig. 3 (a) Map of the round-trip link in SJTU and photo of the 40×10Gb/s coherent UDWDM-PON systems; (b) BER performances versus received optical power for downstream signal at selective channels; (c) BER performances of all the channels at received power of -40 dBm for each channel; (d) BER performance of the downstream signal during 8-hour real-time measurement.

5. Conclusions

We experimentally demonstrate the field trial of a real-time 40×10Gb/s coherent UDWDM-PON system at 5-GHz spacing with power budget of 29 dB after 40-km field-installed transmission. The real-time operation at the OLT and ONU sides are realized by an DSP architecture implemented in FPGAs. The system performance is also evaluated over 8-hour real-time measurement at the receiver power of -40 dBm per channel.

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6. References

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